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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,614	03/31/2000	David W. Grawrock	042390.P8084	2176

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EXAMINER	
ALI, AHMEDUR R	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 11/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,614	GRAWROCK, DAVID W.	
	Examiner	Art Unit	
	Ahmedur Ali	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. The application has been examined. Claims 1-23 are pending in this Office Action

Drawings

2. The drawings are objected to by the draftsperson. A proposed drawing correction or corrected drawings are required in reply to this Office Action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-6 and 8-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Dalvi et al. U.S. Patent No. 6,073,243 ('Dalvi' hereinafter). With respect to claim 1, Dalvi teach a method comprising:

implementing an integrated circuit device within an electronic system, the integrated

circuit device including an override disable pin (see abstract; col. 2, lines 51-53; col. 4, lines 5-25; col. 12, lines 38-52; col. 15, lines 7-10; col. 23, lines 66-67 to col. 24, lines 1-4); and

preventing modification of a representation of a primary pass-phrase when the override disable pin is asserted, the primary pass-phrase permitting access to stored information within the electronic system (see col. 19, lines 1-15; col. 23, lines 20-56, 66-67 to col. 24, lines 1-4).

5. Claim 2 is rejected as above in rejecting claim 1, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device (see Fig. 1; col.3, lines 65-67 to col.4, lines 1-4).

6. Claim 3 is rejected as above in rejecting claim 1, wherein preventing of the modification of the

primary pass-phrase includes

setting a control storage element within the integrated circuit device upon assertion of the override disable pin (see col. 9, lines 38-55); and

disabling modification of the primary pass-phrase when the control storage element is set (see col. 9, lines 38-55; col. 12, lines 48-52).

7. Claim 4 is rejected as above in rejecting claim 3, wherein the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the

primary pass-phase into the electronic system (see col. 23, lines 5-10, 22-25).

8. Claim 5 is rejected as above in rejecting claim 1, wherein the integrated circuit device further

includes an override pin which, when asserted, allows a stored representation of the primary pass-phrase to be modified (see col. 23, lines 51-56).

9. Claim 6 is rejected as above in rejecting claim 1, wherein the preventing of the modification of the primary pass-phrase includes signaling a control application software initiating a request for modification of the pass-phrase that a user is denied access to the stored information of the integrated circuit device unless the primary pass-phrase is correctly entered (see col. 23, lines 5-56).

10. Claim 8 is rejected as above in rejecting claim 1, wherein control storage element includes at least one control register configured for permanent state retention over a plurality of power cycles (see col. 5, lines 16-28; col. 12, lines 20-37).

11. With respect to claim 9, Dalvi teach a method comprising:

enabling access to stored information within an electronic system upon assertion of an override disable pin of an integrated circuit device (see col. 4, lines 5-25; col. 12, lines 38-52; col. 15, lines 7-10; col. 23, lines 66-67 to col. 24, lines 1-4); and

disabling access to the stored information despite assertion of the override pin of the integrated circuit device when an override disable pin of the integrated circuit device is asserted prior to assertion of the override pin (see col. 19, lines 1-15; col. 23, lines 20-56, 66-67 to col. 24, lines 1-4).

12. Claim 10 is rejected as above in rejecting claim 9, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device (see Fig. 1; col. 3, lines 65-67 to col. 4, lines 1-4).

13. Claim 11 is rejected as above in rejecting claim 9, wherein the act of disabling access comprises setting a control storage element within the integrated circuit device in response to the assertion of the override disable pin (see col. 9, lines 38-55); and

determining whether the control storage element is set (see col. 9, lines 38-55; col. 12, lines 53-67).

14. Claim 12 is rejected as above in rejecting claim 11, wherein the control storage element is set after placing the electronic system in an administration mode upon correctly inputting the primary pass-phase into the electronic system (see col. 23, lines 5-31).

15. Claim 13 is rejected as above in rejecting claim 9, wherein the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power cycles (see col. 5, lines 16-28; col. 12, lines 20-37).

16. With respect to claim 14, Dalvi teach a method comprising:

enabling placement of an electronic system into an administrator mode upon assertion of an override disable pin of an integrated circuit device (see col. 4, lines 5-25; col. 12, lines 38-52; col. 15, lines 7-10; col. 23, lines 66-67 to col. 24, lines 1-4); and

disabling placement of the electronic system into the administrator mode despite assertion of the override pin of the integrated circuit device when an override disable pin

of the integrated circuit device is asserted prior to assertion of the override pin (see col. 19, lines 1-15; col. 23, lines 20-56, 66-67 to col. 24, lines 1-4).

17. Claim 15 is rejected as above in rejecting claim 14, wherein the integrated circuit device comprises a package to form a packaged integrated circuit device (see Fig. 1; col. 3, lines 65-67 to col. 4, lines 1-4).

18. Claim 16 is rejected as above in rejecting claim 14, wherein the act of disabling access comprises setting a control storage element within the integrated circuit device in response to the assertion of the override disable pin (see col. 9, lines 38-55); and

determining whether the control storage element is set (see col. 9, lines 38-55; col. 12, lines 53-67).

19. Claim 17 is rejected as above in rejecting claim 14, wherein the setting of the control storage element includes setting a bit of at least one control register configured for permanent state retention over a plurality of power cycles (see col. 5, lines 16-28; col. 12, lines 20-37).

20. With respect to claim 18 Delvi teach an electronic system (see Fig. 1) comprising:

a bus, a processor coupled to the bus, a system memory coupled to the bus, and an integrated circuit device coupled to the bus, the integrated circuit device including (see Fig. 1):

a memory (see Fig. 1),

an override pin to enable access to information stored within the memory upon assertion of the override pin (see col. 19, lines 1-15; col. 23, lines 20-56),

an override disable pin to disable access to the information stored within the memory despite the assertion of the override pin when the override disable pin is asserted prior to assertion of the override pin (see col. 19, lines 1-15; col. 23, lines 20-56, 66-67 to col. 24, lines 1-4).

21. Claim 19 is rejected as above in rejecting claim 18, wherein the integrated circuit further comprises a package to contain the memory from which the override pin and the override disable pin protrude (see Fig. 1).

22. Claim 20 is rejected as above in rejecting claim 18, wherein the memory of the integrated circuit device is non-volatile memory (see col. 1, lines 18-20; col. 6, lines 38-44; col. 15, lines 18-22).

23. Claim 21 is rejected as above in rejecting claim 18, wherein the integrated circuit device further includes a control storage element (see col. 2, lines 54-67).

24. Claim 22 is rejected as above in rejecting claim 21, wherein the control storage element of the integrated circuit device includes at least one control register configured for permanent state retention over a plurality of power cycles (see col. 5, lines 16-28; col. 12, lines 20-37).

25. Claim 23 is rejected as above in rejecting claim 18, wherein the integrated circuit device 2 further includes a microcode to determine whether the override disable pin has been 3 asserted prior to assertion of the override pin (see col. 9, lines 2-7, 38-55).

Claim Rejections - 35 USC § 103

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

27. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dalvi et al. U.S. Patent No. 6,073,243 ('Dalvi' hereinafter) in view of Angelo U.S. Patent No. 5,944,821.

28. With respect to claim 7, Dalvi teach all the limitations as above as indicated in claim 1.

Dalvi do not explicitly disclose a primary pass-phrase that includes a hash value of the primary pass-phrase.

Angelo teaches the representation of the primary pass-phrase includes a hash value of the primary pass-phrase (see col. 3, lines 25-35; col. lines 2-15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Angelo within the teachings of Dalvi to arrive at the invention as claimed because both references are directed to permitting and disabling access to stored information within an electronic system, and the combined teachings would enable the microcode to compare the incoming representation with a pre-stored representation such as comparing the incoming hash value with a pre-stored hash value, further improving the integrity of the primary pass-

phrase and furthermore increasing level of security of the combined system in which the primary pass-phrase may be modified during the administrator mode.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dalvi et al. (U.S. Patent No. 5,954,818) disclose a method of programming, erasing, and reading block lock-bits and a master lock-bit in a flash memory device.

Bergum et al. (U.S. Patent No. 5,457,748) disclose a method and apparatus for improved security within encrypted communication devices.

Bergum et al. (U.S. Patent No. 5,249,227) disclose a method and apparatus of controlling processing devices during power transition.

Chan et al. (U.S. Patent No. 5,978,860) disclose a system and method for disabling and re-enabling peripheral devices in a computer system.

Trostle (U.S. Patent No. 5,919,257) discloses a networked workstation intrusion detection system.

Reardon (U.S. Patent No. 6,212,635) discloses a network security system allowing access and modification to a security subsystem after initial installation when a master token is in place.

Matyas (U.S. Patent No. 5,231,666) discloses a cryptographic method for updating financial records.

Hamdy-Swink (U.S. Patent No. 5,901,284) discloses a method and system for communication access restriction.

Cox et al. (U.S. Patent No. 5,349,643) disclose a system and method for secure initial program load for diskless workstations.

Madany et al. (U.S. Patent No. 5,935,242) disclose a method and apparatus for initializing a device.

Davis (U.S. Patent No. 5,937,063) discloses a secure boot.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ahmedur Ali whose telephone number is 305-4667. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 305-9648. The fax phone number for the organization where this application or proceeding is assigned is 305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-3900.

ara

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